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06EC45

Fourth Semester B.E. Degree Examination, December 2010
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. ***Missing data may be suitably assumed.***

PART – A

1 a. Discuss the needs of HDL. **(06 Marks)**

b. With general syntax and suitable examples, explain the shift operators available in VHDL and verilog. **(12 Marks)**

c. Differentiate between an entity and a symbol. **(02 Marks)**

2 a. What do you mean by the data flow style of description? Explain its features with a suitable example. **(05 Marks)**

b. Write a data flow description VHDL for a system that has three 1-bit inputs a(1), a(2) and a(3); and one 1-bit output b. The least significant bit is a(1); and b is 1, only when (a(1)a(2)a(3)) = 1, 3, 6 or 7 (all in decimal). Otherwise b is 0. Derive a minimized Boolean function of the system and write the data flow description. **(10 Marks)**

c. With a suitable example, explain the concept of signal declaration. **(05 Marks)**

3 a. With syntax of CASE statement in VHDL and verilog, discuss its facts. **(10 Marks)**

b. Write a behavioral description of a 4-bit binary counter, in verilog. **(10 Marks)**

4 a. Write a VHDL structural description for full adder, using two half adders. **(06 Marks)**

b. What is the advantage of structural coding in verilog, compared to structural coding in VHDL? **(02 Marks)**

c. Define state machine. Using the state machine concept, showing all the details, design a counter, which counts 0, 2, 3, 5, 7 . Write the VHDL code for the same. (Use JK flip-flop). **(12 Marks)**

PART – B

5 a. With declaration syntax of procedure, explain its facts. **(08 Marks)**

b. Write a verilog function to find the largest of the two signed numbers. **(08 Marks)**

c. Bring out the differences between functions and procedures. **(04 Marks)**

6 a. What do you understand by a file in HDL? List out the VHDL procedures for file processing. **(04 Marks)**

b. With syntax, explain the package and the package body. **(06 Marks)**

c. Write VHDL code for the state diagram shown in figure Q6 (c). **(10 Marks)**

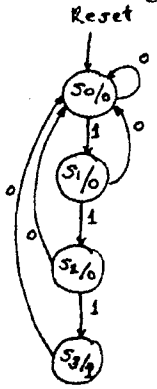

Fig. Q6 (c)

7 a. Discuss the facts and limitations of mixed language description. **(08 Marks)**

b. With mixed language description of full adder, explain the invoking of VHDL entity from a verilog module. **(12 Marks)**

8 a. Define synthesis. **(02 Marks)**

b. With a neat flow chart, explain the steps involved in a synthesis process. **(08 Marks)**

c. Draw the gate level synthesis information, extracted from the following verilog code.

```
always @ (s, a, b)
begin
    if (s = = 1'b1)
      Y = b;
    else
      Y = a;
end
```

(05 Marks)

d. Explain the mapping of the signal assignment statement, $y \Leftarrow x$; to gate level, with a suitable example. **(05 Marks)**

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